Remarks

Upon entry of the foregoing amendment, claims 11-23 and 25-26 are pending in the application, with claims 11 and 18 being the independent claims. Claim 18 and 25 are sought to be amended to further clarify the invention. Support for the amendments to claims 18 and 25 are found in specification at: page 153, lines 15-35; page 154, lines 1-10; and FIGs. 75-78. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Advisory Action mailed March 29,2006

The Advisory Action alleges that there is no support for the claim amendments filed on 3/13/06. Specifically, the Advisory Action alleges there is no support in the specification for "the adjusting step including reducing a drain source voltage across the variable gain amplifier for increasing amplitude of the input signal voltage." Applicant traverses below.

The Amendment, filed 3/13/06, specifically recited support for the amendment in the first paragraph of the Remarks section of the Amendment. "Support for the amendments to claims 18 and 25 are found in specification at: page 153, lines 15-35; page 154, lines 1-10; and FIGs. 75-78. " Accordingly, the Examiner is referred to these pages of the Specification as providing support for the amendment. Even more specifically, page 153, lines 21-29, recite,

> " In the first method of Vas control, gain and linearity in the output of the VGA tend to be controlled by adjusting each of four transistors' M4, M10, M13, M14 drain source voltages ("V_{ds}") of the transistors to control a

> transductance ("g_m") associated with each transistor. If a drain source voltage V_{ds} across a MOSFET device M10, M4, M13, M14 ***is reduced***, a g_m transfer characteristic of that transistor, which is a function of input voltage, ***becomes flatter***. The ***flatter the g_m transfer function*** the ***more linearly*** the transistor tends to operates." (*emphasis added*)

Based on the above recitations, Applicant asserts that there is sufficient support for the claim amendments filed on 3/13/06. Accordingly, Applicant requests entry of the amendment and reconsideration and allowance of the pending claims.

The Amendments and Remarks section of the amendment filed on 3/13/06 is repeated herewith for convenience.

Rejections Under 35 U.S.C. § 112

On pages 2, claims 18 stands rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Specifically, the recitation "generating a voltage control signal based on an amplitude of the input signal voltage", is allegedly to not clearly be described in the specification.

Applicant's disagree that the mentioned recitation is not sufficiently described in the specification for purposes of 35 U.S.C. § 112, second paragraph, and point to the following in the specification for support: page 151, lines 5-10; page 152, lines 7-12, and the discussion of FIG. 77 in the specification.

However, in order to expedite prosecution, Applicant has deleted the mentioned recitation from claim 18, rendering this rejection moot. Accordingly, Applicant requests that the rejection under 35 U.S.C. § 112, second paragraph, be reconsidered and withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 18-22 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated over U.S. Pat. No. 5,955,921 to Ide *et al* (hereinafter "Ide") Applicant respectfully disagrees and traverses this rejection.

Claim 18 includes the features of:

> adjusting a transconductance of the variable gain amplifier in response to the input signal voltage *so as to flatten a transconductance transfer characteristic* of the variable gain amplifier...
>
> (See, claim 18, *emphasis added*)

Ide does not teach or suggest *flattening a transconductance transfer characteristic of the variable gain amplifier in response to the input voltage signal*, as recited in claim 18. The Office Action allegedly points to FIG. 8, and column 16, lines 55-60 of Ide. Applicants agree that FIG. 8 illustrates an AGC amplifier, but the mentioned portion of Ide only states that the "gain control transistor pair 39 controls a ratio of current values flowing in the two transistor pairs 37,38, thereby varying a transconductance value of the entire AGC amplifier circuit 27." (*See*, Ide, col 16, lines 55-60).

Even though Ide discloses *varying a transconductance value* as shown above, Ide makes no mention of *flattening a transconductance transfer characteristic of the variable gain amplifier in response to the input voltage signal*, as recited in Applicant's claim 18. The Examiner is reminded that the current rejection is an anticipation rejection, which requires that "each and every element as set forth in the claim [be] found either expressly or inherently described, in a single prior art reference." (*See*, MPEP 2131, citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F. 2d 628, 631).

Clearly Ide does not teach *flattening a transconductance transfer characteristic.* Accordingly, based the discussion above, Ide does not teach each and every feature of the

claimed invention, and therefore Applicant requests that the rejection under 35 U.S.C. 102(e) be removed and that claim 18 be passed to allowance.

Further claim 18 was further amended for clarification of the invention to recite that:

> *the adjusting step including reducing a drain source voltage across the variable gain amplifier for increasing amplitude of the input signal voltage.*
> (See, claim 18, *emphasis added*)

Ide does not teach the recited feature of *reducing a drain source voltage across the variable gain amplifier for increasing amplitude of the input signal voltage*, nor does the Office Action allege this. Specifically, Ide does not teach or suggest in FIG. 8 and the related specification, *reducing* the drain source voltage of FET devices 37A, 37B, 38A, or 38B for *increasing* input signal amplitude in order to flatten the transconductance curve, as is recited in Applicant's claim 18. Nor, does the Office Action allege this. Accordingly, Ide does not teach each and every feature of claim 18, and therefore does not anticipate claim 18. Accordingly, Applicants request that the rejection under 35 U.S.C. 102(e) be removed and that claim 18 and its respective dependent claims 19-22, and 25-26 be passed to allowance.

Rejections Under 35 U.S.C. § 103

Claim 23 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ide. Applicant respectfully disagrees and traverses this rejection.

Claim 23 depends from independent claim 18, which is was indicated to be allowable over Ide based on the discussion above. Accordingly, claim 23 should also be patentable over Ide for being dependent from an allowable base claim, in addition to its own patentable features.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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